OPTIMUM DESIGN OF DIFFERENTIAL LOW NOISE AMPLIFIER USING MULTI OBJECTIVE GENETIC ALGORITHM

***Rafal R. mahmood**[1] , **Dr Ahmad T. younis**[2]
[1,2] *Department Electronic Eng*
Ninevah University
Mosul, Iraq
[1]*rafal.mahmod@uoninevah.edu.iq*, [2]*Ahmad.younis@uonineval.edu.iq*

Abstract: *Low Noise Amplifier (LNA) plays an important role in most modern wireless communication systems. This paper presents an optimum design for Differential Low Noise Amplifier (DLNA) operates at 5 GHz. The most important parameter that include minimum noise figure (NF), maximum gain and minimum power consumption are to be satisfied and obtained. Multiple Objective Genetic Algorithm (MOGA) is used and implemented using Matlab software. There are many realization topologies that LNAs are designed and realized]. A differential LNA topology is selected to be optimized and simulated using (MOGA) since differential topology offers a certain preferred performance LNA parameter. An improved performance is obtained that include increasing gain (23.65dB), reducing NF (1.6dB) and reducing power consumption(12.58mw).*

Keywords : LNA, ADS, MATLAB, Multi -objective Genetic algorithm

1. INTRODUCTION

Wireless communication system such as remote receivers, WLANs and mobile phones, applications operate from 2 to 5 GHz. The first stage of an RF receiver is generally the Low Noise Amplifier (LNA). Its primary purpose is to reduce the noise figure of later stages and to get an adequate gain. In addition, it should show a specific impedance to the input source such as 50Ω [1], [2].

The significance of LNA lies in the fact that they influence the noise performance as much as all the other partitions in the receiver chain [3]. The Low Noise Amplifier (LNA) is the compulsory front-end component between the antenna and the mixer in any Radio Frequency (RF) receiver design. As LNA is the receiver's very front end level, the main performance parameters to be affected and must be considered are noise figure (NF), gain and power consumption[4].

During the LNA design process, designers confront the issue of trade-off quantities such as noise figure, gain, power consumption, input / output matching and linearity. An optimum LNA would result from the right balance of all these design quantities [3].

This paper presents a differential LNA topology due to many well-known features such as immune responses to common mode distortions, rejection of parasite couplings and improved dynamic range, differential topology is generally chosen in RF design.[5].

An optimization procedure may be an appropriate way to avoid the design challenges and to meet and satisfy the required performance of the LNA. The optimization technique of the genetic Aalgorithm (MOGA) is based on the natural evolution

process to obtain the optimum parameters of a problem. Moreover, the multi objective genetic algorithm is capable of solving and optimizing nonlinear and complex systems[6].

2. Mathematical Design of DLNA

The differential LNA topology contains two similar single stage amplifier as shown in Figure. 1

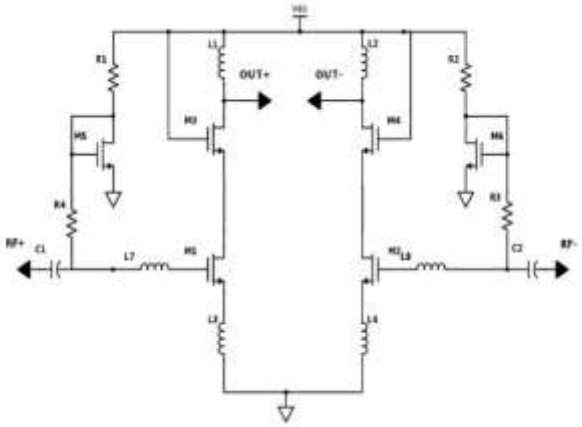


Figure. 1. Differential LNA topology

The LNA design must meet the performance requirements specified for the most important component values. These could include the W1, W2 and W3 transistor widths. Inductor values LS, Lg, Ld, CL, CB coupling capacitance, and current biasing Id [7] .Thus, the differential structure can be designed first by treating the single stage as shown in Figure. 2 and then combined both stage to provide differential operator [8].

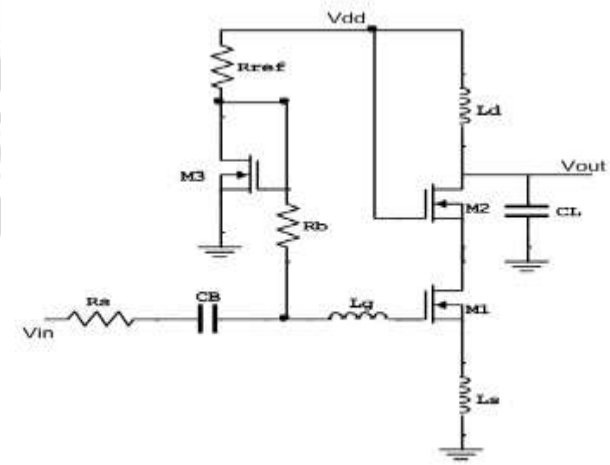


Figure. 2 .single ended LNA topology

The design is completed for 5GHz operating frequency under fabrication process of 0.18µm [2].
µ0=293.168,Tox=4.1*$\mathbf{10^{-9}}$,Ɛ0=8.854*$\mathbf{10^{-12}}$,Ɛr=3.9 for Sio2 , VDD=1.8V , Id =5mA

Cox=(Ɛ0* Ɛr–)/Tox =8.422*10^-3

- The device width of transistor MOSFET1 (M1) and MOSFET2 (M2) are determined by

$$W_1=\frac{3}{2*C_{ox}*L_1*Q_{opt}*w_0*}=161.522\mu m \quad (1)$$

- The Gate to source capacitor C_{gs} is calculated as :

$$C_{gs}=\frac{2}{3}*C_{ox}*W_1*L_1=0.16PF \quad (2)$$

- Trans-conductance (g_{m1}) of MOSFET1 (M1) is given as :

$$g_{m1}=\sqrt{2*\mu_n*C_{ox}*\frac{W}{L}I_d}=47.076$$

- Therefore the transistor unity gain frequency W_T (3)

$$W_T=\frac{g_m}{C_{gs}}=294GHz \quad (4)$$

- The values of L_s , L_g , and L_d are obtained as follows:

$$Ls=\frac{R_S}{W_T}=0.17nH \quad (5)$$

$$Lg=\frac{1}{W_0{}^2*C_{gs}}-Ls=6.33nH \quad (6)$$

$$L_d=\frac{1}{W_0{}^2*C_L}=2.04nH \quad (7)$$

- Then the voltage gain can be determined as:

$$A_V=\frac{gm1}{Cgs*W0}=12dB \quad (8)$$

- The minimum noise figure is given as:

$$NF = \left(1 + 2.4 * \frac{w_0}{W_T}\right) = 1.24 \quad (9)$$

- The power dissipation is then calculated to be:

$$P_D = 2 * I_d * V_{DD} = 18\text{mw} \quad (10)$$

In the design analysis, it is assumed that the width of the transistors (M1 , M2) in cascode amplifier is equal $(\frac{W}{L})_1 = (\frac{W}{L})_2$. The ratio of the cascode transistor is the same with the ratio of the common source stage. The width and current of the bias transistor are arbitrarily selected as one tenth of that of the CS transistor. $(\frac{W}{L})_3 = (\frac{1}{10})(\frac{W}{L})_1$ [5].

GA optimization of Differential LNA

The aim of applying GA on this LNA topology is to obtain optimum design values that provide improved performance parameters of NF, gain and power consumption.

The main transistors are M2 and M1 while the transistors for cascoding are M4 and M3. The inducers of degeneration include L6 and L5. The blocking capacitors that can also be used off-chip are C2 and C1. The widths of the transistors M1, M2, M4 and M3 are maintained to be the same in order to preserve symmetry. For biasing, the transistors M6 and M5 are used. The transistor M1 and M6 are also used as current mirrors. To provide the correct bias current .The width of the biasing transistor M5 is modified to be one tenth of the main transistor and provide the suitable biasing current.

In attempting to obtain the frequency of resonances, the gate inductor (L8, L7) and the degenerated inductor (source inductor) (L4, L3) play an important role. The measurements of these inductors are therefore adjusted in such a way as to provide the frequency resonant at which the device must operate [8] .Two drain inductors LD are applied to match the output impedance [5].The amplifier gain, NF and power consumption are designed to be objective parameters that formulate the fitness function are given as shown in **Table 1.**

Table 1. Fitness Function and Constraint

Specifications/Constraints	Type	Equation
noise figure	Fitness Function	(9)
gain	Fitness Function	(8)
power dissipation	Fitness Function	(10)
Gate to source capacitor Cgs	Constraint	(2)
L_s degeneration inductor	Constraint	(5)
L_g inductance at the gate	Constraint	(6)

A general GA flowchart is illustrated in Figure 3 The most important steps of the algorithm are the creation of the initial population, the assessment of the fitness function and the creation by the application of the genetic operators of a new population of individuals: selection, recombination and mutation[9].

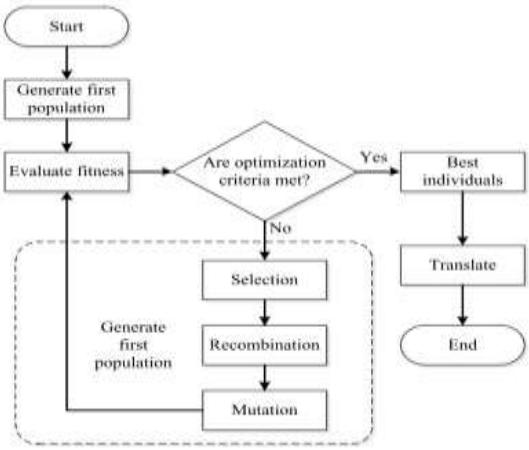


Figure 3. General GA

A tradeoff between minimization power consumption, minimization noise figure and maximization gain is employed and it is based on (MOGA). The NSGA-II (Non dominated Sorting Genetic Algorithm II) is incorporated into the GA toolbox proposed by[10]. This method has shown good results in solving complex multi-objective optimization problems, and has been able to discover various solutions to the Pareto front with little computational effort[9].The flowchart shown in Figure 3 illustrated the steps used for optimization using MATLAB language MOGA multi-objective Genetic Algorithm toolbox. the design variables that are selected to be (Id, width W1) the chromosome is designed to contain these variables that illustrate in

.

Table 2. Design variables limit using MOGA

Variables name	***values***
W1	10 to 500 um
ID	1 to 10 mA

In other hand (Ls, Lg, Cgs) are used as nonlinear constraint function to obtain minimization for power consumption and noise figure, maximization gain, and to satisfy the required specifications and performances that illustrate in **Table 3** and

Table .

Table 3 . LNA specifications design target for 0.18um CMOS process

Parameter name	**Value**
Frequency (GHz)	5
Supply Voltage(V)	1.8
S22(dB)	< -10
S11(dB)	< -10
S21 (dB)	> 10
Noise Figure(dB)	< 3
Power consumption(mW)	< 15
Source/load Impedance (Ω) Values	50

Table 4. Constraints limit using MOGA

Constrained	**values**
LS	0.1 to 10 nH
Lg	1 to 50 nH
Cgs	0.05 to 10 pF

Table present the GA based on MOGA result compared with that obtained analytically. It can be shown from this figure that a significant improvement is obtained in transistor dimension power consumption, and amplifier gain. However, it can be seen that this improvement is a price of increasing the noise figure, this is the concept of tradeoff between variables.

Table 5 . Comparison between optimization using MOGA and the mathematical method

design parameters and performance	**Differential low noise amplifier**	
	mathematical	***Optimized using GA***
Width W_1	161.522	98.26µm
I_d	5 mA	3.49mA
C_{gs}	0.163	0.0973PF
g_m	47.07	48ms
L_S	0.17	0.1nH
L_g	6.33	10.04nH
L_d	2.04	0.66nH
NF	1.54dB	1.6dB
POWER CONSUMPTION	18mw	12.58mw

Power GAIN S21	12.16dB	23.65dB

3. COMPARISON BETWEEN MOGA AND OTHER EXISTING TECHNIQUES:

The benefit of applying MOGA is shown as a further comparison between the multi-objective genetic algorithm presented in this work and other existing techniques. Although the comparison applies to various technologies and other parameters, it still provides a good indication of the gain, noise figure (NF) and power consumption improvements achieved using the GA strategy. Table 6. demonstrates, among other techniques, the benefits of using MOGA.

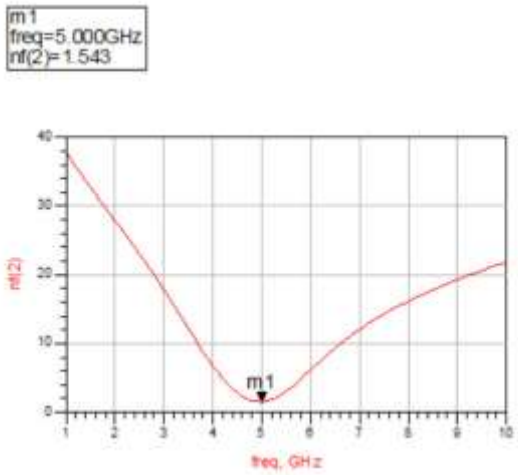
Table 6. Comparison between MOGA results and other techniques:

Parameters	[8]	[11]	[12]	[13]	THIS WORK
LNA Technology	***Differential***	***Cascode CS***	***Cascode CS***	***Fully-differential***	***Differential using MOGA***
Process(nm)	UMC 180 nm CMOS	180	180	130	180
Supply Voltage(V)	1.8	1.5	0.6	1.2	1.8
Frequency (GHz)	2.4	5	5	5.0	5
S11(dB)	-13.5	-10	-14	-25	-12.07
S22(dB)	-10	-12	-16	-12	
S21(dB)	12.68	9.3	12.5	18	23.65
S12(dB)	-33.85			-28	-33.7
NF(dB)	3.14	2.8	4.5	2.62	1.6dB
Power Consumption		30	0.32	10.3	12.58mw

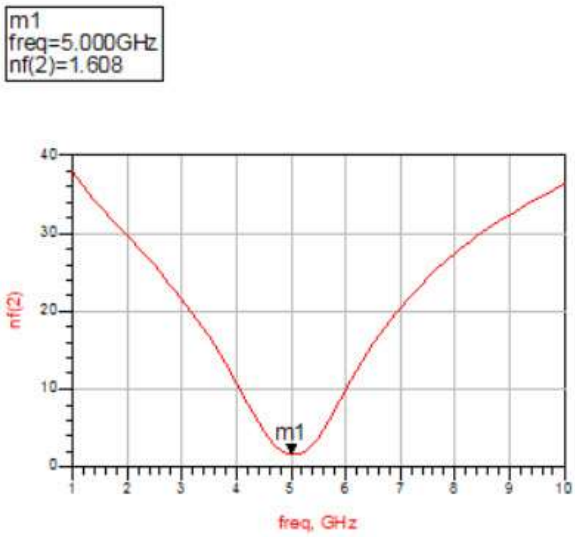
4. SIMULATION RESULTS

The differential LNA topology with its circuit parameters obtained from MOGA is applied and simulated using Advanced Design System (ADS) environment. The designed operating frequency is 5GHz realized using 0.18µm CMOS technology.

Figure 4. and Figure 5. Present the simulation results for noise figure, gain and power consumption respectively.it can be illustrated from these figures that a good agreement between designed and simulated result are obtained.

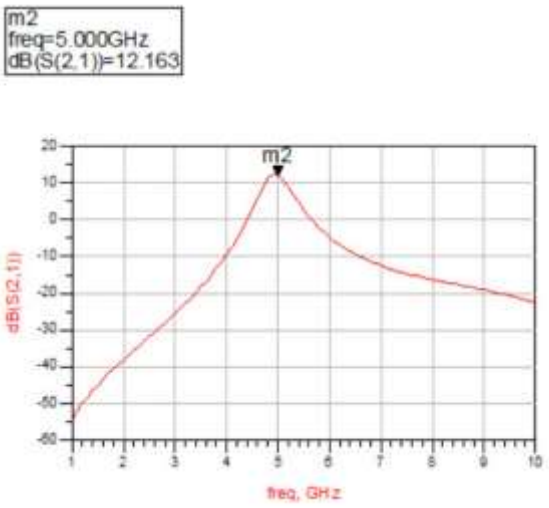


(a)mathematical

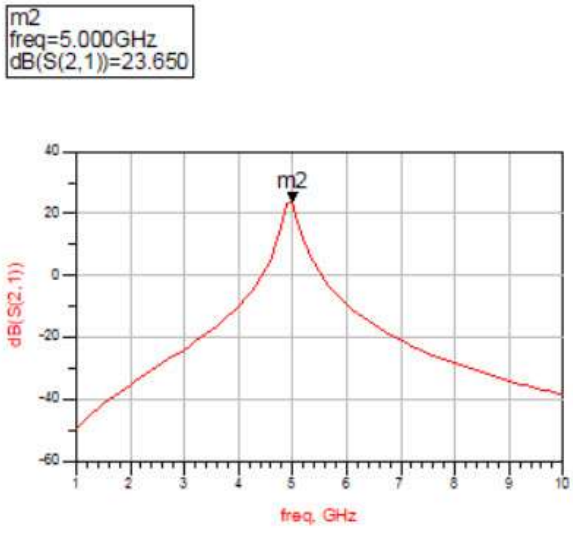


(b)optimized

Figure 4. Simulated results for noise figure mathematical and optimized values



(a) mathematical



(b)optimized

Figure 5. Simulated results power gain S21 figure mathematical and optimized values

5. Conclusions

Multi Objective Genetic Algorithms (MOGA) is employed and realized in matlab to improve Differential low noise amplifier DLNA performance. A 5 GHz Differential low noise amplifier DLNA is designed, optimized and simulated to satisfy the required specifications.

Multi Objective Genetic Algorithms (MOGA) is used to minimize NF, minimize power consumption and maximize gain. A significant important on these performance parameters were obtained NF=1.6dB and power consumption=12.58mw and gain =23.65dB .

Simulation results using ADS were presented and showed a good agreement with that designed.

References

[1] T. H. Lee, The design of CMOS radio-frequency integrated circuits. Cambridge university press, 2003.

[2] T. Kanthi and D. Sharath Babu Rao, "Design And Analysis Of CMOS Low Noise Amplifier Circuit For 5-GHz Cascode and Folded Cascode In 180nm Technology," Int. J. Reconfigurable Embed. Syst., vol. 7, no. 3, p. 149, 2018, doi: 10.11591/ijres.v7.i3.pp149-156.

[3] A. Papadimitriou and M. Bucher, Multi-objective Low-Noise Amplifier Optimization Using Analytical Model and Genetic Computation, vol. 36, no. 12. Springer US, 2017.

[4] D. Submitted, T. H. Fulfillment, T. Degree, and E. Engineering, "ANALYSIS OF IMPACT OF TRANSFORMER COUPLED INPUT MATCHING ON CONCURRENT DUAL-BAND LOW," 2011.

[5] S. Adiloğlu et al., "Design Concepts of Low-Noise Amplifier for Radio Frequency Receivers," Intech, vol. i, no. tourism, p. 13, 2012, doi: 10.1016/j.colsurfa.2011.12.014.

[6] A. T. Younis and E. A. Abdo, "LOW NOISE AMPLIFIER (LNA) PERFORMANCE OPTIMIZATION USING GENETIC ALGORITHMS (GA S)," vol. XX, no. 5, pp. 1–11, 2020.

[7] M. Iyer and T. Shanmuganantham, "Design of Low Noise Amplifier for 802.16e," Lect. Notes Networks Syst., vol. 46, no. October 2011, pp. 823–838, 2019, doi: 10.1007/978-981-13-1217-5_82.

[8] N. Shrivastava and R. Khatri, "Design of a 2.4-GHz differential low noise amplifier using 180nm technology," Int. Conf. Recent Innov. Signal Process. Embed. Syst. RISE 2017, vol. 2018-Janua, pp. 494–497, 2018, doi: 10.1109/RISE.2017.8378206.

[9]J. J. Roberts, A. M. Cassula, J. L. Silveira, and P. O. Prado, "GAtoolbox: a Matlab - based Genetic Algorithm Toolbox for Function Optimization," 12th LATIN-AMERICAN Congr. Electr. Gener. Transm. - CLAGTEE 2017, pp. 1–12, 2017.

[10]K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan, "A fast and elitist multiobjective genetic algorithm: NSGA-II," IEEE Trans. Evol. Comput., vol. 6, no. 2, pp. 182–197, 2002, doi: 10.1109/4235.996017.

[11]D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," IEEE J. Solid-State Circuits, vol. 32, no. 5, pp. 745–759, 1997.

[12]C. L. Hsieh, M. H. Wu, J. H. Cheng, J. H. Tsai, and T. W. Huang, "A 0.6-V 336-μW 5-GHz LNA using a low-voltage and gain-enhancement architecture," IEEE MTT-S Int. Microw. Symp. Dig., vol. 2, pp. 6–8, 2013, doi: 10.1109/MWSYM.2013.6697468.

[13]Y. W. Hsiao and M. D. Ker, "An ESD-protected 5-GHz differential low-noise amplifier in a 130-nm CMOS process," Proc. Cust. Integr. Circuits Conf., no. Cicc, pp. 233–236, 2008, doi: 10.1109/CICC.2008.4672066.